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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/727,319
Filing Date: December 03, 2003
Appellant(s): HUANG ET AL.

Mitch Harris
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is a ***supplemental response*** to the appeal brief filed December 19, 2006 appealing from the Office action mailed August 28, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

5,404,543 A	Faucher et al.	04-1995
6,128,641 A	Fleck et al.	10-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 3, 10 and 11 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 8-10, 16 and 18-19 of copending Application No. 10/727,320 (hereinafter referred to as '320) in view of Faucher et al. (U.S. Patent No. 5,404,543) (hereinafter referred to as Faucher). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

In re claim 1, claim 16 of co-pending application '320 meets all the limitations of claim 1 of the instant application except, co-pending application '320 does not explicitly claim the invention further comprising: an output port coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller; and an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller.

Faucher teaches a memory controller (20) that comprises usage evaluator(s) (power management machine 66) that comprise: an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller

within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57); and an input port (access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller (Faucher discloses information about the state of all of the memory banks being restored within the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24). Faucher has the additional benefit of reducing power within the system memory (column 1, lines 39-49).

It would have been obvious to one of ordinary skill of the art having the teachings of the '320 and Faucher at the time the invention was made, to modify the memory controller of claim 1 of '320 to include input and output ports coupled to the usage evaluators as taught by Faucher. One of ordinary skill in the art would be motivated to make this combination of including input and output ports coupled to the usage evaluators in view of the teachings of Faucher, as doing so would give the added benefit of reducing power consumption within the system memory (as taught by Faucher above).

Claim 3 of the instant invention is identical to claim 18 of '320.

Re claim 10, claim 8 of co-pending application '320 meets all of the limitations of claim 10 of the instant application except co-pending application '320 does not explicitly claim the invention wherein said device controller further includes: an output port coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator by said processor, whereby a state of said at least one usage evaluator may be stored in said memory by said processor; and an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator by said processor, whereby said state of said at least one usage evaluator may be restored from said memory.

Faucher teaches a memory controller (20) that comprises usage evaluator(s) (power management machine 66) that comprise: an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57); and an input port (access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least

one usage evaluator may be restored from information stored external to said device controller (Faucher discloses information about the state of all of the memory banks being restored within the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24). Faucher has the additional benefit of reducing power within the system memory (column 1, lines 39-49).

It would have been obvious to one of ordinary skill of the art having the teachings of the '320 and Faucher at the time the invention was made, to modify the memory controller of claim 8 of co-pending application '320 to include input and output ports coupled to the usage evaluators as taught by Faucher. One of ordinary skill in the art would be motivated to make this combination of including input and output ports coupled to the usage evaluators in view of the teachings of Faucher, as doing so would give the added benefit of reducing power consumption within the system memory (as taught by Faucher above).

Claim 11 of the instant invention is identical to claim 9 of '320.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Faucher et al. (U.S. Patent No. 5,404,543) (hereinafter referred to as Faucher).

As to claim 1, Faucher discloses a device controller (memory controller 20) for coupling (via bus 42) one or more controlled devices (memory modules 30 of memory bank 22) to one or more processors (system CPU 12 and main CPU machine 54) in a processing system (column 3, lines 33-42 and column 3, line 51 thru column 4, line 3 and column 4, lines 25-57), comprising: a command unit (system memory machine 60) for sending commands (RAS and CAS) to said one or more devices (via control bus 36; column 4, lines 25-40 and column 5, lines 54-66); at least one usage evaluator (power management machine 66) having an input coupled (via control bus 36) to an output of said command unit (60) for evaluating a frequency of use of an associated controlled device (Faucher discloses the power management machine [66] comprising counters [one associated for every memory module 30] to establish the "length of time" [hence frequency], since a memory module [30] was used; column 7, lines 38-58); and control logic (power management machine 66) coupled to said usage evaluator (The power management machine [66] and power management scoreboard [64] disclosed by Faucher comprises the functionality listed for both said usage evaluators and control logic as state above) and further coupled to an input of said command unit (Faucher discloses the command unit [system memory machine 60] accommodating various cycles in correlation with control logic [power management machine 66] which necessitates the coupling of these two to each other; column 5, lines 56-61) for sending power management commands in response to said usage evaluator detecting is that a

usage level of said associated device has fallen below a threshold level (pre-established time period), whereby said device controller power manages (alters voltage delivered to memory modules [30]) said controlled device without intervention by said one or more processors (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21) (Though Faucher does not explicitly recite the power managing mode altered in relation to a usage level falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that memory module will be placed into a lower power mode by decreasing the voltage level to the memory module); an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru

column 7, line 16 and column 7, lines 38-57); and an input port (access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller (Faucher discloses information about the state of all of the memory banks being restored within the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24).

As to claim 3, Faucher discloses the device controller wherein said device controller is a memory controller, and wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40).

As to claim 4, Faucher discloses the device controller wherein said at least one usage evaluator comprises an inter-arrival time counter for determining an interval between accesses to said associated memory module (column 7, lines 38-58).

As to claim 5, Faucher discloses the device controller further comprising one or more power management control registers (70, 72 and 74), each associated with a particular one of said one or more controlled devices (column 6, lines 10-55 and column 7, lines 3-16), each coupled to an input port of said device controller and further coupled to said command unit, whereby a power management control state for said associated controlled device can be set by

said one or more processors (54) and set in said associated controlled device by said device controller (column 5, lines 13-24).

As to claim 6, Faucher discloses the device controller wherein said power management control registers are further coupled to said at least one usage evaluator, whereby values of said power management control registers are adjusted in conformity with a result of said evaluating (steps 108, 116, 120, 128 and 134 in figures 5 and 6 reveal the scoreboard [54] being updated after changes made).

As to claim 7, Faucher discloses the device controller wherein said evaluator further comprises an adaptive threshold circuit for adjusting said threshold in response to said evaluated frequency of use of said one or more controlled devices (Faucher discloses changing a threshold [time-out value] dependent on whether system is operating on AC or DC power; column 6, lines 48-55).

As to claim 8, Faucher discloses the device controller wherein said one or more controlled devices include a counter for determining a level of usage of each controlled device during a current process, and wherein said device controller further comprises another input port coupled to each of said controlled devices for reading a value of said counter, and wherein said control logic updates said at associated evaluator in conformity with said value of said counter (column 7, lines 38-58).

As to claim 9, Faucher discloses the device controller wherein said device controller is a memory controller, wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40) incorporating usage counters (column 7, lines 41-45), and wherein said control logic is coupled to said command logic whereby said

control logic periodically reads current counts from said memory modules (column 4, lines 25-57).

As to claim 10, Faucher discloses a processing system (10), comprising: a processor (system CPU 12 and main CPU machine 54); a memory (memory bank 22 consisting of memory modules 30) coupled to said processor for storing program instructions and data values (column 3, lines 33-42 and column 4, lines 25-40); a device controller (memory controller 20) coupled to said processor (column 3, lines 33-50); one or more controlled devices (memory modules 30 within memory bank 22) coupled to said device controller (via buses 32, 34 and 36; column 4, lines 25-40), wherein said controlled devices (memory modules 30) have multiple power management states (column 1, lines 39-49), and wherein said device controller (memory controller 20) includes a command unit (system memory machine 60) for sending commands (RAS and CAS) to said one or more devices (via control bus 36; column 4, lines 25-40 and column 5, lines 54-66), at least one usage evaluator (power management machine 66) having an input coupled (via control bus 36) to an output of said command unit for evaluating a frequency of use of an associated controlled device (column 7, lines 38-58), and control logic (power management machine 66) coupled to said usage evaluator (The power management machine [66] and power management scoreboard [64] disclosed by Faucher comprises the functionality listed for both said usage evaluators and control logic as state above) and further coupled to an input of said command unit (Faucher discloses the command unit [system memory machine 60] accommodating various cycles in correlation with control logic [power management machine 66] which necessitates the coupling of these two to each other; column 5, lines 56-61) for sending power management commands in response to said usage evaluator detecting that a usage level of

said associated device has fallen below a threshold level (pre-established time period), whereby said device controller power manages said controlled device without intervention by said processor (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21) (Though Faucher does not explicitly recite the power managing mode altered in relation to a usage level falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that memory module will be placed into a lower power mode by decreasing the voltage level to the memory module); and wherein said device controller further includes an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator by said processor, whereby a state of said at least one usage evaluator may be stored in said memory by said processor (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru

column 7, line 16 and column 7, lines 38-57); and an input port (access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator by said processor, whereby said state of said at least one usage evaluator may be restored from said memory (Faucher discloses information about the state of all of the memory banks being restored within the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24).

As to claim 11, Faucher discloses the processing system wherein said device controller is a memory controller, and wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40).

As to claim 13, Faucher discloses the processing system wherein said at least one usage evaluator comprises an inter-arrival time counter for determining an interval between commands sent to said associated controlled device (column 7, lines 38-58).

As to claim 14, Faucher discloses the processing system wherein said device controller further comprises one or more power management control registers (70, 72 and 74), each associated with a particular one of said one or more controlled devices (column 6, lines 10-55 and column 7, lines 3-16), each coupled to an input port of said device controller and further coupled to said command unit, whereby a power management control state for said associated

controlled device can be set by said processor (54) and set in said associated controlled device by said device controller (column 5, lines 13-24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 15 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faucher (as cited above) in view of Fleck et al. (U.S. Patent No. 6,128,641) (hereinafter referred to as Fleck).

As to claim 15, Faucher discloses a method of managing power in a processing system (column 1, lines 39-49), comprising: sending power management setting information for devices (memory modules 30 of memory bank 22) controlled by a device controller (memory controller 20) to said device controller (column 4, lines 25-57); evaluating a usage (track length of time since last access via counters) of each of said controlled devices (memory modules 30 of

memory bank 22) within said device controller (via power management machine [66] found within memory controller [20]) in order to determine whether or not said usage has fallen below a threshold (Though Faucher does not explicitly recite the power managing mode altered in relation to a frequency falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that memory module will be placed into a lower power mode by decreasing the voltage level to the memory module; column 7, lines 38-58 and column 13, line 67 thru column 14, line 21); sending power management commands ("number of inputs from memory controller") from said device controller to said controlled devices (via programmable memory power system [24]; column 3, line 51 thru column 4, line 3) in conformity with a result of said determining, whereby said device controller manages a power management state of said controlled devices without processor intervention (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21).

Faucher does not explicitly disclose receiving an indication of a context switch activating a second process and deactivating a first process; and in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch receiving an indication of a context switch activating a second process and deactivating a first process; and

in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch.

Fleck teaches a data processing unit that comprises register file (2), system memory (1) and an instruction control unit (3) to assist in context switching. Fleck further teaches receiving an indication of a context switch activating a second process and deactivating a first process; and in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch receiving an indication of a context switch activating a second process and deactivating a first process; and in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch (Fleck teaches a first context state being preserved in memory when second context state is initiated. Fleck further teaches the first context state being restored once the second context state is completed; column 1, line 45 thru column 2, line 45). Fleck has the additional feature of decreasing memory space needed and reducing execution overhead (column 1, lines 28-35).

It would have been obvious to one of ordinary skill of the art having the teachings of Faucher and Fleck at the time the invention was made, to modify the power managing method of Faucher to include saving and recovering context switch states as taught by Fleck. One of ordinary skill in the art would be motivated to make this combination of include saving and recovering context switch states in view of the teachings of Fleck, as doing so would give the added benefit of decreasing memory space needed and reducing execution overhead (as taught by Fleck above).

As to claim 18, Faucher in combination with Fleck taught the power managing method in claim 15, as shown above. Fleck further teaches the method further comprising retrieving usage

counts from said controlled devices, and wherein said evaluating is performed in conformity with said retrieved usage counts (column 3, line 56 thru column 4, line 5).

As to claim 19, Faucher in combination with Fleck taught the power managing method in claim 15, as shown above. Faucher further teaches the method further comprising adjusting said threshold in accordance with a result of said evaluating, whereby said evaluating is made adaptive to said usage (Faucher discloses changing a threshold [time-out value] dependent on whether system is operating on AC or DC power; column 6, lines 48-55).

As to claim 20, Faucher in combination with Fleck taught the power managing method in claim 15, as shown above. Faucher further teaches the method wherein said device controller is a memory controller, wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40), wherein said sending sends power management setting information to said memory modules, and wherein said evaluating determines a frequency of accesses to said memory modules (column 7, lines 41-45) (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21) (Though Faucher does not explicitly recite the power managing mode altered in relation to a usage level falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that

memory module will be placed into a lower power mode by decreasing the voltage level to the memory module).

(10) Response to Argument

As reminded by the Appellant, independent claim 1 (and similarly independent claim 10) recites:

> *A device controller for coupling one or more controlled devices to one or more processors in a processing system, comprising:*
> *a command unit for sending commands to said one or more devices;*
> *at least one usage evaluator having an input coupled to an output of said command unit for evaluating a frequency of use of an associated controlled device;*
> *control logic coupled to said usage evaluator and further coupled to an input of said command unit for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level, whereby said device controller power manages said controlled device without intervention by said one or more processors;*
> *an output port coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller; and,*
> *an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller.*

Faucher discloses (as clearly shown in drawings below):

- A device controller (**B. of Fig. 2**) for coupling one or more controlled devices (**C. of Fig. 2**) to one or more processors (**A. of Fig. 2**) in a processing system (column 3, line 3 thru column 4, line 57).

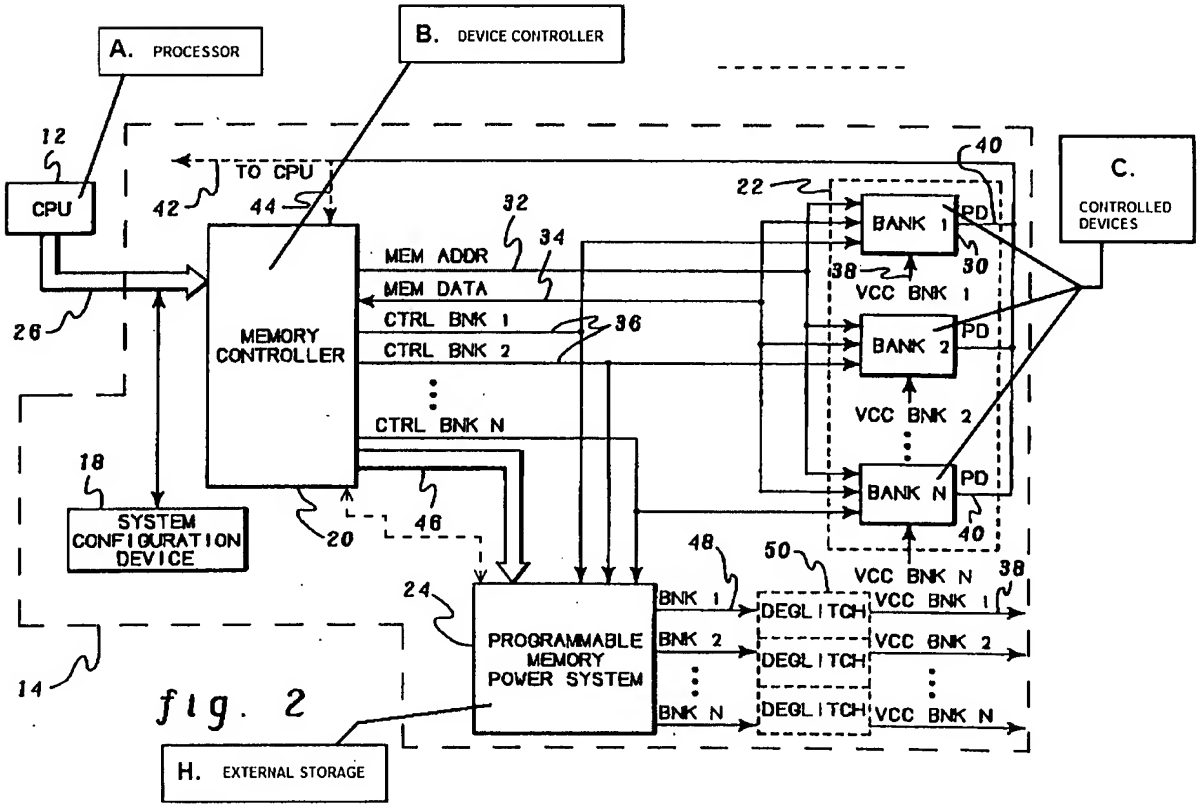


fig. 2

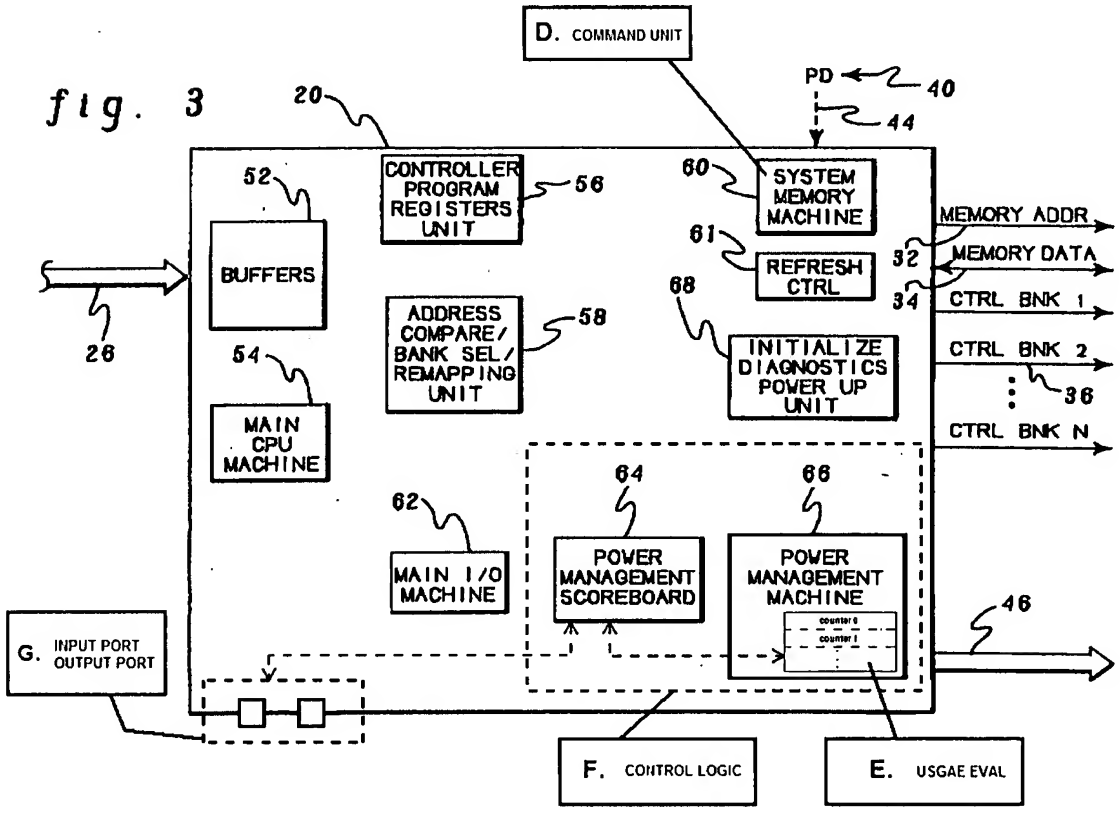
- a command unit (**D. of Fig. 3**) for sending commands to said one or more devices (column 4, lines 25-40 and column 5, lines 54-66).
- at least one usage evaluator (**E. of Fig. 3**) having an input coupled to an output of said command unit for evaluating a frequency of use of an associated controlled device (column 5, line 54 thru column 6, line 20 and column 7, lines 38-58).

Faucher discloses the power management machine 66 comprising counters associated with each bank (controlled device) within the memory system to keep track of memory bank usage according to the length of time since last access. Usage amount is then stored within 105 of 64 which is described below.

- control logic (units 64 and 66 of Faucher are herein combined to create **F. of Fig. 3** shown by dotted box) coupled to said usage evaluator and further coupled to an input of said command unit (inherently necessitates being coupled to command unit since command unit **D** acts upon comparison result from **F**) for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level ("pre-established time period"), whereby said device controller power manages said controlled device without intervention by said one or more processors (column 7, lines 38-58 and column 13, line 67 thru column 14, line 21).
- an output port (**G. of Fig. 3**) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external (within **G. of Fig. 2**) to said device controller; and, an input port (**G. of Fig. 3**) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external (within **G. of Fig. 2**) to said device controller (column 2, lines 16-24 and column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57). Faucher teaches the device

controller **(B. of Fig. 2)** comprising computer interfaces which is synonymous with an input port and an output port. Faucher further teaches the usage evaluators **(E)** evaluating the frequency since the last access to a memory bank and storing the timer status (105) within the scoreboard (which is within control logic **F**). Faucher further discloses state data stored within scoreboard 64 of control logic **F** is *updated from* and *stored to* the programmable memory power system 24 (external storage **G**) of the memory system which necessitates coupling as noted by dotted lines within Fig. 3 below and Fig. 2 above.

fig. 3



In short, the **usage evaluators (counters E)** in machine 66 evaluate usage of the memory banks. This usage indicator is stored within the scoreboard 64. The state data stored within the

scoreboard is stored to and updated from the **external storage (H)** which necessitates the **usage evaluators (E)** being indirectly coupled to an input port and an output port.

I. Faucher does not disclose the invention of Claims 1, 3-11, 13 and 14.

Appellant argues that Faucher does not disclose "*an output port and input port for reading and setting a state of the usage evaluator so that the state can be stored and restored external to the device controller*" (APPEAL BRIEF, page 6, lines 13-17).

The Examiner stands by the rejection presented as Faucher does disclose an output port and an input port for reading and setting a state of the usage evaluator so that the state can be stored and restored external to the device controller. Faucher teaches the device controller (**B. of Fig. 2**) comprising computer interfaces which is synonymous with an input port and an output port. Therefore, Faucher *does disclose* the mere presence of the input/output port. Further, Faucher states that "state data" stored within the scoreboard 64 is stored to and updated from the external storage **H** as shown in Fig. 2 above. This necessitates communicating over the ***computer interfaces*** (ports) as shown hereinabove.

The Appellant continues to argue "the selected voltage is not the 'state' of the usage evaluator itself in the context of the present invention" and is not associated with the usage evaluators (APPEAL BRIEF, page 7, lines 14-22). It is noted that the features upon which applicant relies (i.e., "the state of a usage evaluation can be preserved, ... , for each thread across thread execution slices and is described in the exemplary embodiment as the state of the inter-arrival counts and/or statistics of usage evaluators"; APPEAL BRIEF, page 8, lines 1-6) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification,

limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). All that is claimed is that the "state" of the usage evaluator (stored within the scoreboard 64) and stored external to the device controller which is disclosed in Faucher.

Also, independent claim 1, in re the "input port" and "output port", uses the phrases "coupled to" and "may be" which constitutes a use limitation. This language renders the claims indefinite as to what structure is embraced by the metes and bounds of the claim language. See MPEP § 2111.04.

Therefore, the Examiner's rejection of claims 1, 3-11, 13 and 14 under 35 USC § 102(b) as being anticipated by Faucher remains standing.

Furthermore, the Examiner would like to assert that the Appellant has had ample opportunity to amend the claims to include the limitations argued above but has failed to do so. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

II. Faucher in view of Fleck does not disclose or suggest the invention of Claims 15 and 18-20.

The Applicant argues and disagrees with the rejection to claims 15 and 18-20 under 35 USC § 103(a) as being unpatentable over Faucher in view of Fleck for the reasons argued that Faucher does not disclose the invention as recited. For the same reasons argued above, in re claims 1, 3-11, 13 and 14, the Examiner disagrees and stands by the rejection under 35 USC § 103(a).

III. Faucher does not make obvious Claims 1, 3, 10 and 11 in view of the invention recited in Claims 8-10 of co-pending U.S. Patent Application 10/727,320.

For the same reasons indicated above with respect to the rejections under 35 USC § 102(b), Faucher ***does disclose*** the input and output ports for saving and restoring the state of usage evaluators as cited in the claims. Therefore, the provisional obviousness-type double-patenting rejection remains standing.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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